



Product Specification

M240HVN01.0 Open Cell

AU Optronics Corporation

 Preliminary Specification Final Specification

Module	24.0" Color TFT-LCD
Model Name	M240HVN01.0 Open Cell

Customer

Date

Approved by

Date

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Note: This Specification is subject to change
without notice.

Desktop Display Business Group /
AU Optronics Corporation



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Records of Revision



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1 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 10) Avoid touching COF position while doing mechanical design.
- 11) While storing modules as spares for a long time, the following precautions are necessary:
 - Store modules in a dark place. Do not expose them to sunlight or fluorescent light.
 - Keep the temperature between 5°C and 35°C at normal humidity.



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2 General Description

This specification applies to the 24 inch-FHD color a-Si open cell M240HVN01. The display supports the FHD - 1920(H) x 1080(V) screen format and 16.7M colors (RGB 8-bit data). The light source of this TFT-LCD module is W-LED. All input signals are 2-channel LVDS interface.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

Items	Unit	Specification
Screen Diagonal	[mm]	609.6 (24.0")
Active Area	[mm]	531.36 (H) x 298.89 (V)
Pixels H x V		1920(x3) x 1080
Pixel Pitch	[um]	276.75 (per one triad) x 276.75
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		VA Mode, Normally Black
Optical Response Time	[msec]	12 (Typ., on/off)
Nominal Input Voltage VDD	[Volt]	+ 5.0 V
Power Consumption (VDD line)	[Watt]	4.5 watt (Typ. without inverter, all white pattern @ 60Hz)
Cell Weight	[g]	550 gram (Typ.)
Electrical Interface		Dual channel LVDS
Support Color		16.7M colors (RGB 8-bit)
Surface Treatment		Glare
Cell Transmittance		4.15%
Cell Thickness	[mm]	1.43



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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C:

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree]	Horizontal (Right)	75	89	-	1
		CR = 10 (Left)	75	89	-	
		Vertical (Up)	75	89	-	
		CR = 10 (Down)	75	89	-	
Response Time	[msec]	Rising Time (TrR)	-	7	-	2
		Falling Time (TrF)	-	5	-	
		Rising + Falling	-	12	-	
Crosstalk (in 60Hz)	[%]				1.5	3
Flicker	dB				-20	4



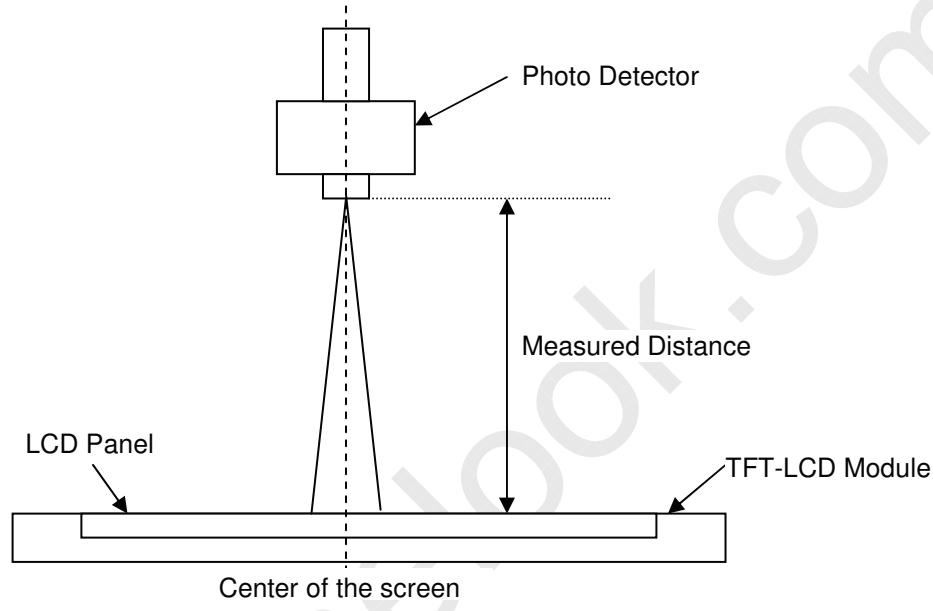
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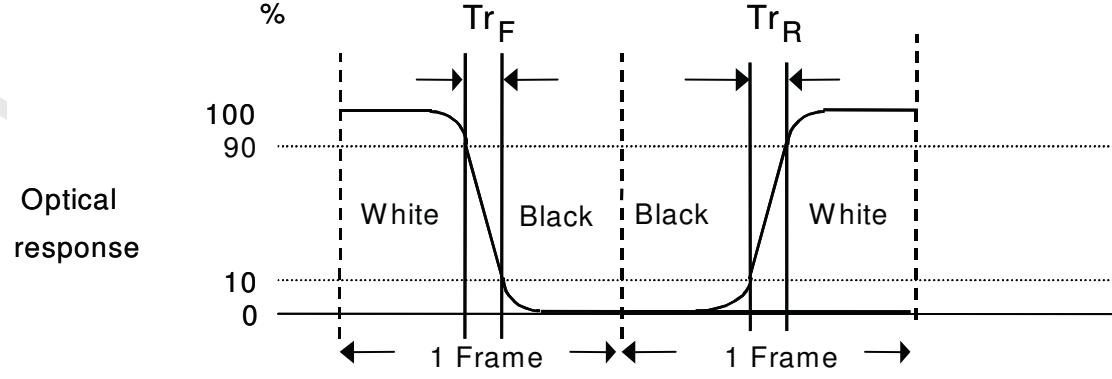
Note 1: Measurement Method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring (at surface 35 °C). In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 2: Response Time measured by Westar TRD-100A

The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time, TrR), and from "Full White" to "Full Black" (falling time, TfF), respectively. The response time is interval between the 10% and 90% (1 frame at 60 Hz) of amplitudes.



$TrR + TfF = 12 \text{ msec (typ.)}$.



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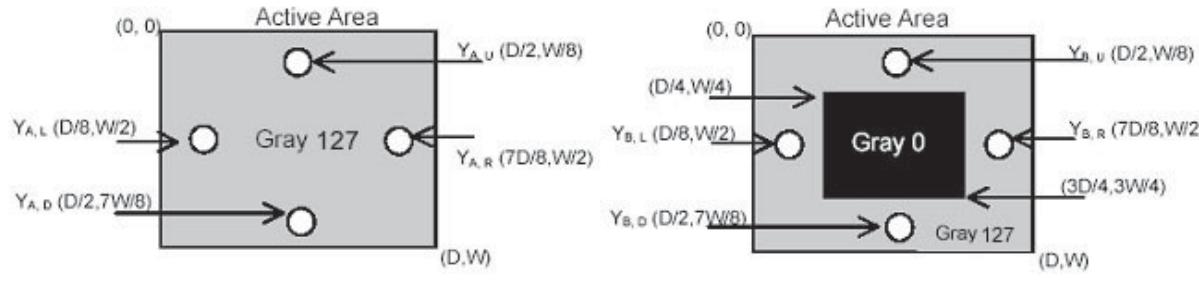
Note 3: Crosstalk defined as below and measured by TOPCON SR-3

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

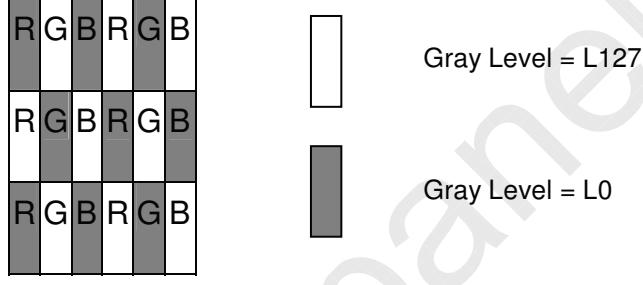
Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

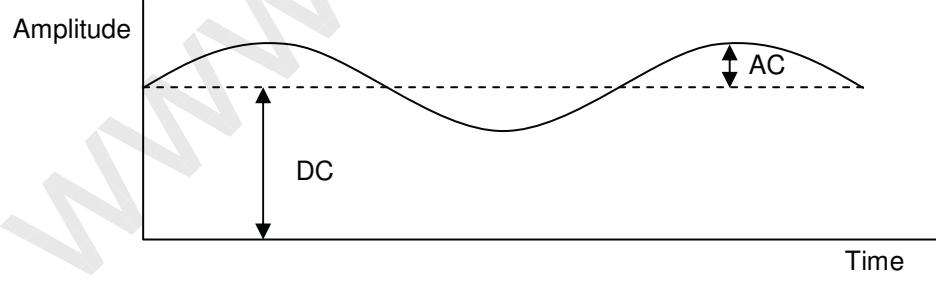
Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note 4: Test Pattern Sub-checker Pattern measured by TOPCON SR-3



Method: Record dBV & DC value with TRD-100



$$\text{Flicker (dB)} = 20 \log \frac{\text{AC Level(at 30 Hz)}}{\text{DC Level}}$$



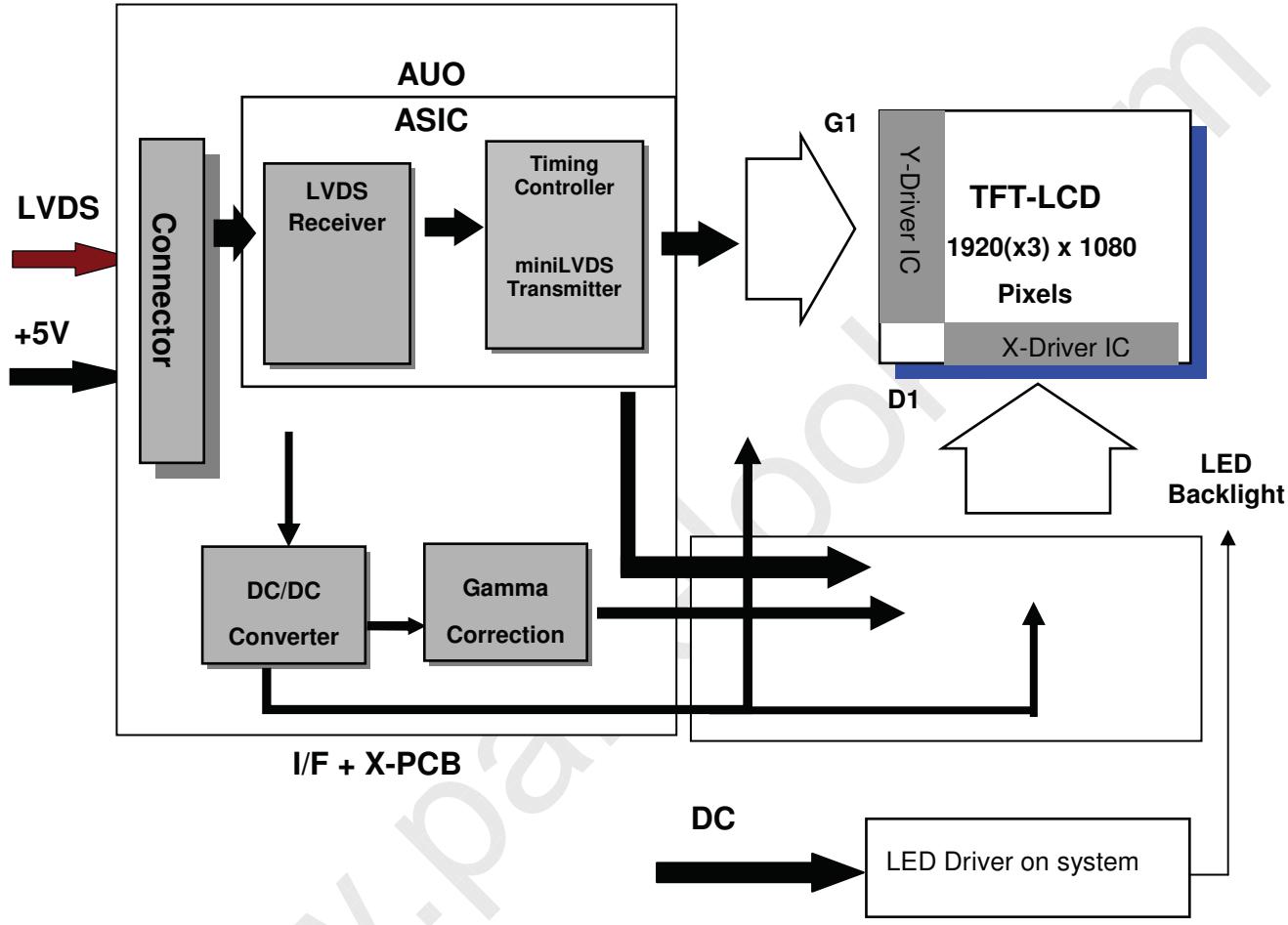
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3 Functional Block Diagram

The following diagram shows the functional block of the 24.0 inch Color TFT-LCD open cell:



I/F PCB Interface:

FI-XPB30SRLA-HF11
01-187121-30091-3(A)

Mating Type:

FI-X30HL(Locked Type)



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4 Absolute Maximum Ratings

Absolute maximum ratings of the open cell are listed as follows:

4.1 TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	VDD	0	6.0	[Volt]	Note 1, 2

4.2 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Glass Surface Temperature (Operation)	TGS	0	+65	[°C]	Note 3 Note 4
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	Note 3

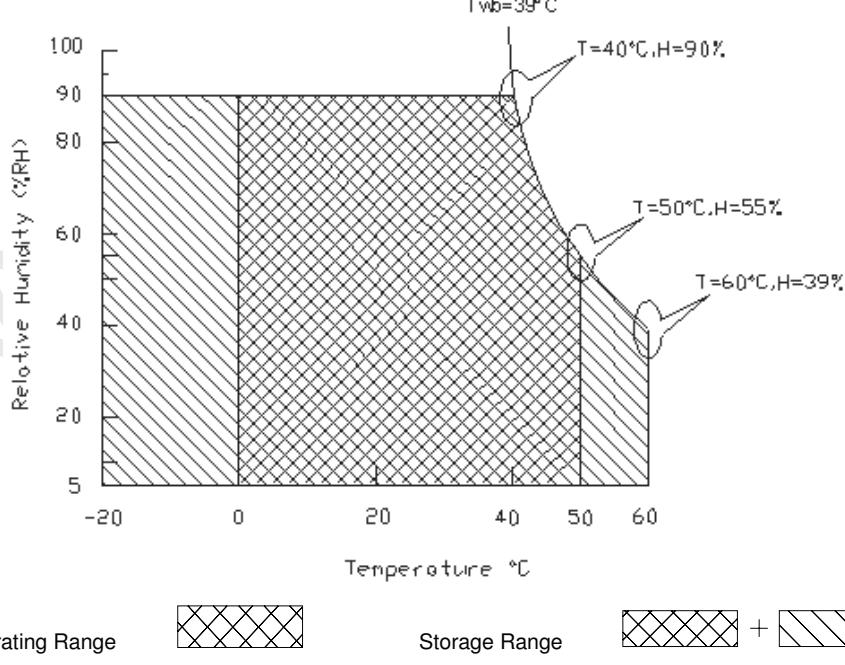
Note 1: With in Ta (25 °C)

Note 2: Permanent damage to the device may occur if exceeding maximum values

Note 3: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta \leq 39°C)
2. Max wet-bulb temperature at 39°C or less. (Ta \leq 39°C)
3. No condensation

Note 4: Function Judged only



Operating Range



Storage Range





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5 Electrical Characteristics

5.1 TFT LCD Open Cell

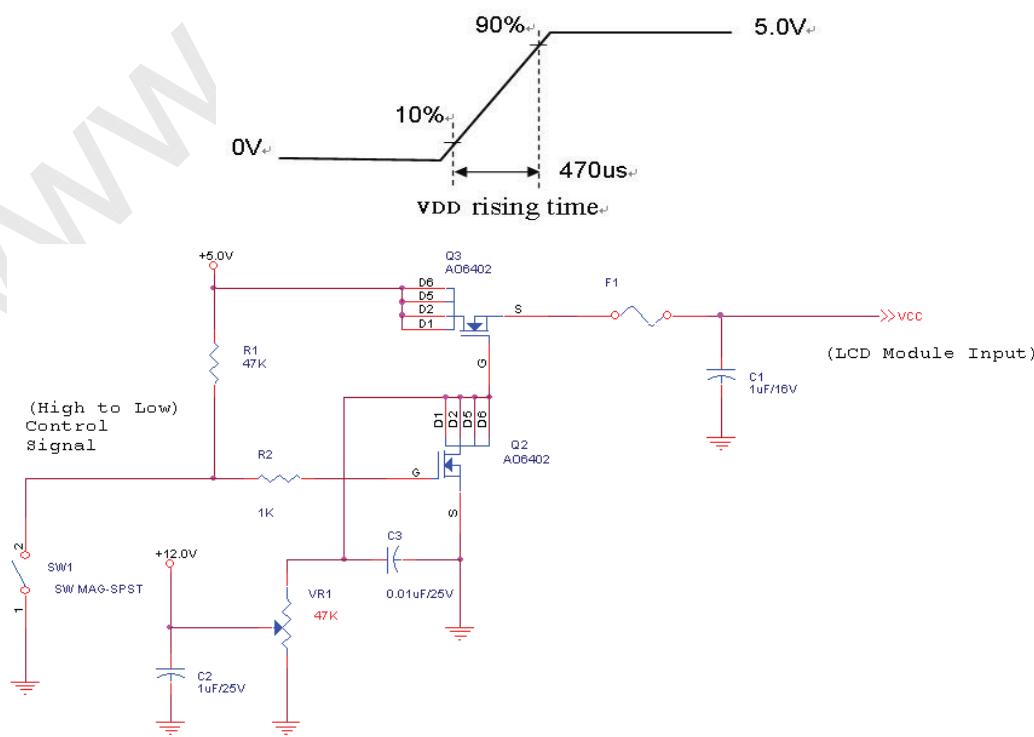
5.1.1 Power Specification

Input power specifications are listed as follows:

Symbol	Description	Min	Typ.	Max	Unit	Conditions
VDD	Logic/LCD Drive Voltage	4.5	5.0	5.5	[Volt]	+/-10%
IDD1	Input Current	-	0.9	1.2	[A]	VDD= 5.0V, All White Pattern at 60 Hz
		-	1.0	1.25	[A]	VDD= 5.0V, All White Pattern at 75 Hz
PDD1	VDD Power	-	4.5	6	[Watt]	VDD= 5.0V, All White Pattern at 60 Hz
		-	5.0	6.35	[Watt]	VDD= 5.0V, All White Pattern at 75 Hz
IRush	Inrush Current	-	-	3	[A]	Note 1
VDDRp	Allowable Logic/LCD Drive Ripple Voltage	-	-	500	[mV] p-p	VDD= 5.0V, All White Pattern at 75 Hz

Note 1: Measurement Conditions:

The duration of rising time of power input is 470 us.





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5.1.2 Signal Electrical Characteristics

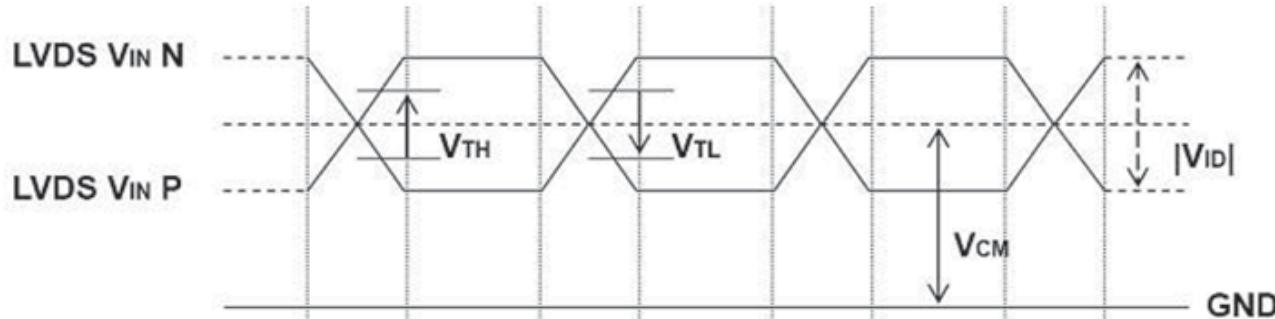
Input signals shall be low or Hi-Z state when VDD is off. Please refer to specifications of SN75LVDS82DGG (Texas Instruments) in detail.

- Characteristics of each signal are listed as follows:

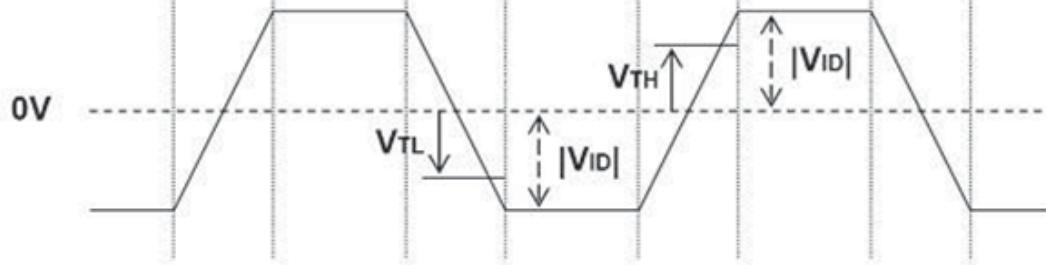
Symbol	Description	Min	Typ	Max	Units	Conditions
VTH	Differential Input High Threshold	-	+50	+100	[mV]	VICM = 1.2V Note 1
VTL	Differential Input Low Threshold	-100	-50	-	[mV]	VICM = 1.2V Note 1
VID	Input Differential Voltage	100	-	600	[mV]	Note 1
VICM	Differential Input Common Mode Voltage	+1.0	+1.2	+1.5	[V]	VTH-VTL = 200mV (max) Note 1

Note 1: LVDS Signal Waveform

Single-End



Differential Signal





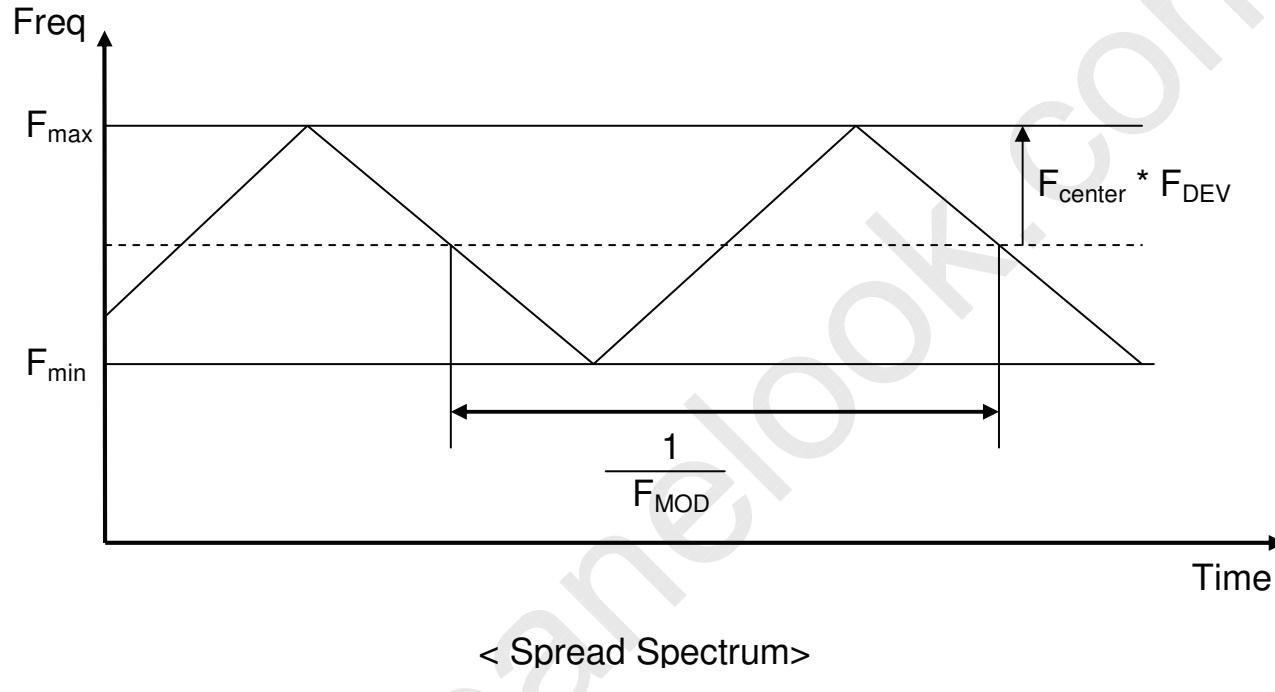
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2) AC Characteristics

Symbol	Description	Min	Max	Units	Conditions
F_{DEV}	Maximum deviation of input clock frequency during SSC	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during SSC	-	200	KHz	





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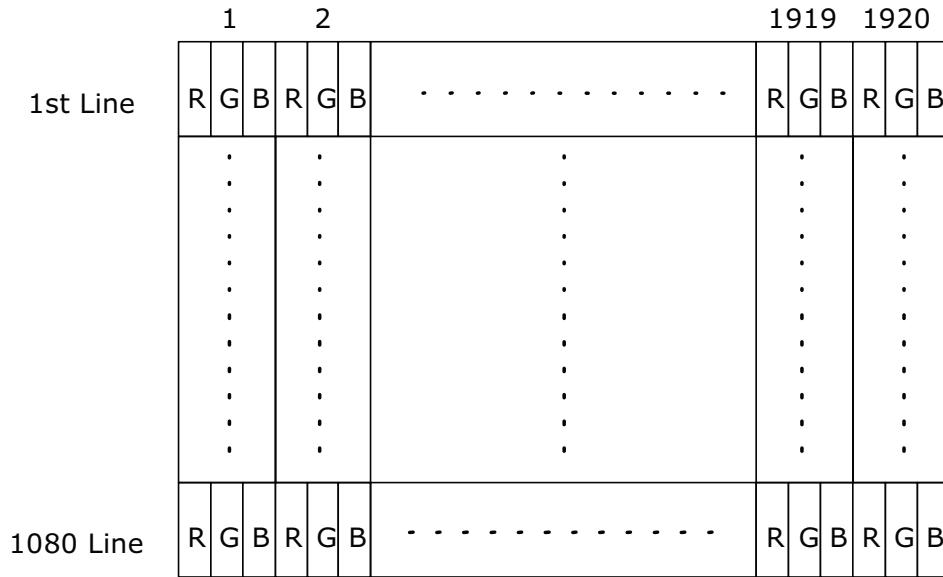
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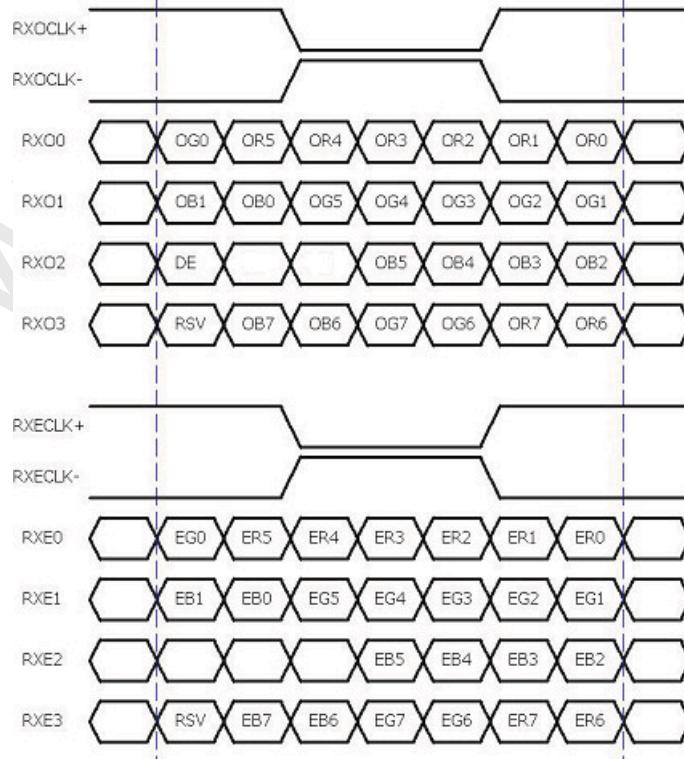
6 Signal Characteristics

6.1 Pixel Format Definition

Following figure shows the relationship between the input signals and LCD pixel format.



6.2 Input Data Format Definition



Note 1: R/G/B data 7:MSB, R/G/B data 0:LSB O = "Odd Pixel Data" E = "Even Pixel Data"



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6.3 Signal Description

The open cell uses one LVDS receiver SN75LVDS82 (Texas Instruments). LVDS is a differential signal technology and high speed data transfer interface for LCD device. LVDS transmitter shall be SN75LVDS83 (negative edge sampling). The first LVDS port (RxOxxx) transmits odd pixels while the second LVDS port (RxExxx) transmits even pixels.

PIN #	Signal Name	Description
1	RxOIN0-	Negative LVDS differential data input (Odd data)
2	RxOIN0+	Positive LVDS differential data input (Odd data)
3	RxOIN1-	Negative LVDS differential data input (Odd data)
4	RxOIN1+	Positive LVDS differential data input (Odd data)
5	RxOIN2-	Negative LVDS differential data input (Odd data, DSPTMG)
6	RxOIN2+	Positive LVDS differential data input (Odd data, DSPTMG)
7	GND	Power Ground
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)
10	RxOIN3-	Negative LVDS differential data input (Odd data)
11	RxOIN3+	Positive LVDS differential data input (Odd data)
12	RxEIN0-	Negative LVDS differential data input (Even data)
13	RxEIN0+	Positive LVDS differential data input (Even data)
14	GND	Power Ground
15	RxEIN1-	Positive LVDS differential data input (Even data)
16	RxEIN1+	Negative LVDS differential data input (Even data)
17	GND	Power Ground
18	RxEIN2-	Negative LVDS differential data input (Even data)
19	RxEIN2+	Positive LVDS differential data input (Even data)
20	RxECLK-	Negative LVDS differential clock input (Even clock)
21	RxECLK+	Positive LVDS differential clock input (Even clock)
22	RxEIN3-	Negative LVDS differential data input (Even data)
23	RxEIN3+	Positive LVDS differential data input (Even data)
24	GND	Power Ground
25	NC	No connection (for AUO test only. Do not connect)
26	NC	No connection (for AUO test only. Do not connect)
27	NC	No connection (for AUO test only. Do not connect)
28	VDD	Power +5V
29	VDD	Power +5V
30	VDD	Power +5V

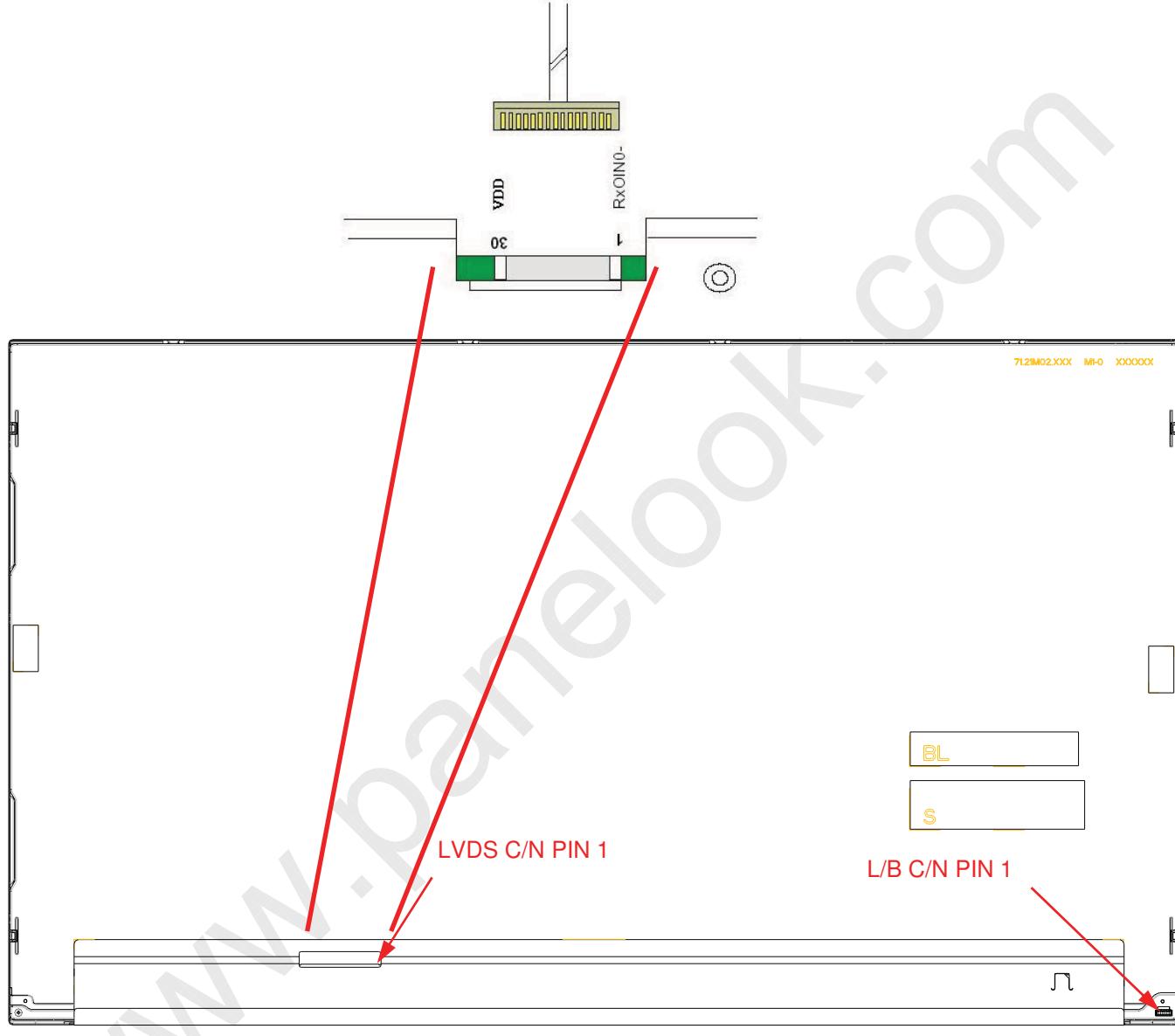


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Note 1: LVDS connector Pin 1 starts from right side, and light bar connector Pin 1 starts from left side.



Note 2: Input signals of odd and even clock shall be the same timing.



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6.4 Timing Characteristics

Basically, interface timing described here is not actual input timing of LCD open cell but close to output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

Item	Symbol	Min	Typ	Max	Unit
Data CLK	Tclk	40	72	90 [Note 2]	[MHz]
H-section	Period	Th	1034	1060	[Tclk]
	Display Area	Tdisp(h)	960	960	[Tclk]
	Blanking	Tblk(h)	74	100	[Tclk]
V-section	Period	Tv	1088	1120	[Th]
	Display Area	Tdisp(v)	1080	1080	[Th]
	Blanking	Tblk(v)	8	40	[Th]
Frame Rate	F	50	60	75	[Hz]

Note 1: DE mode only

Note 2: Spread spectrum on customers' side included

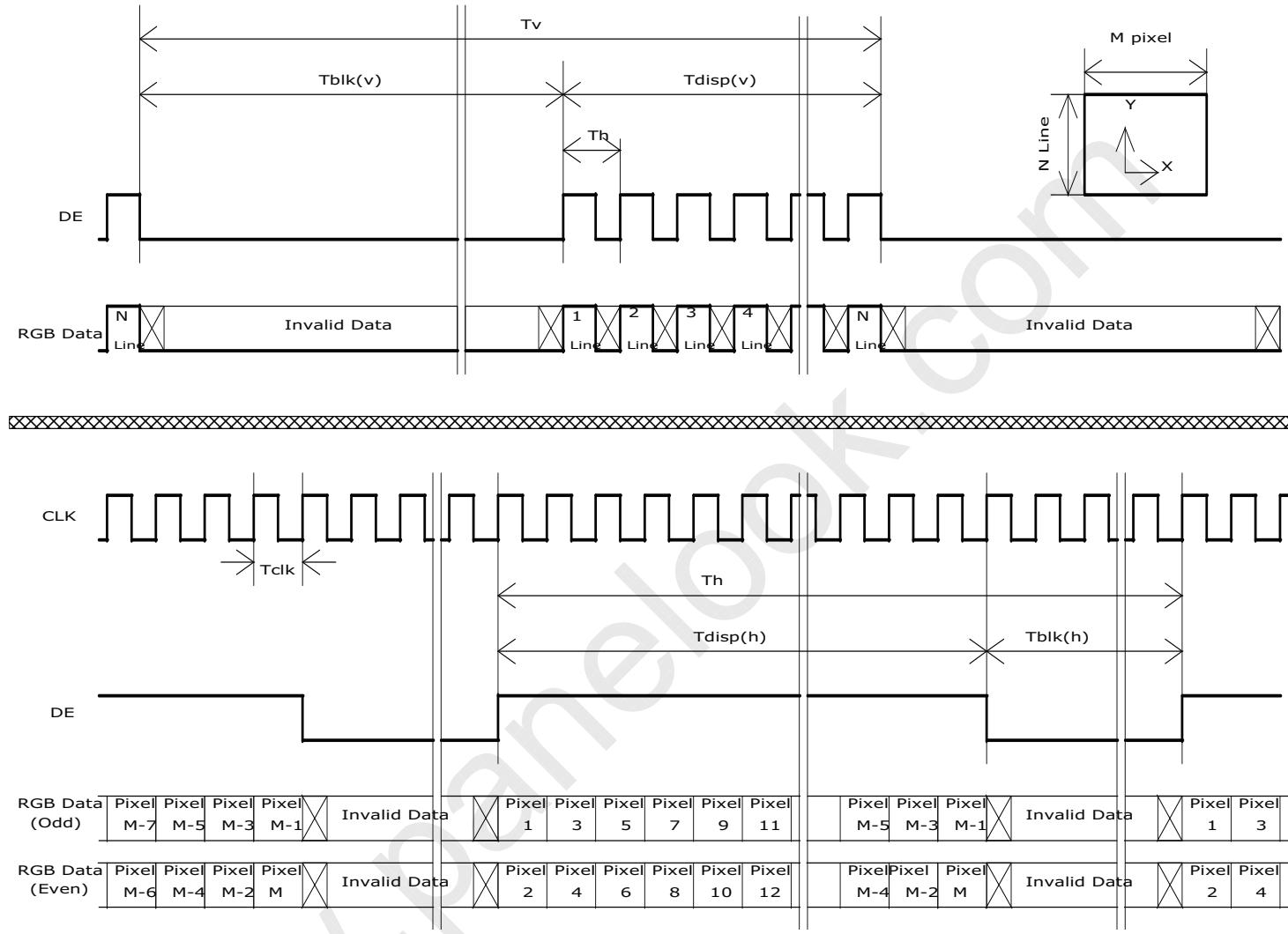


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6.5 Timing Diagram





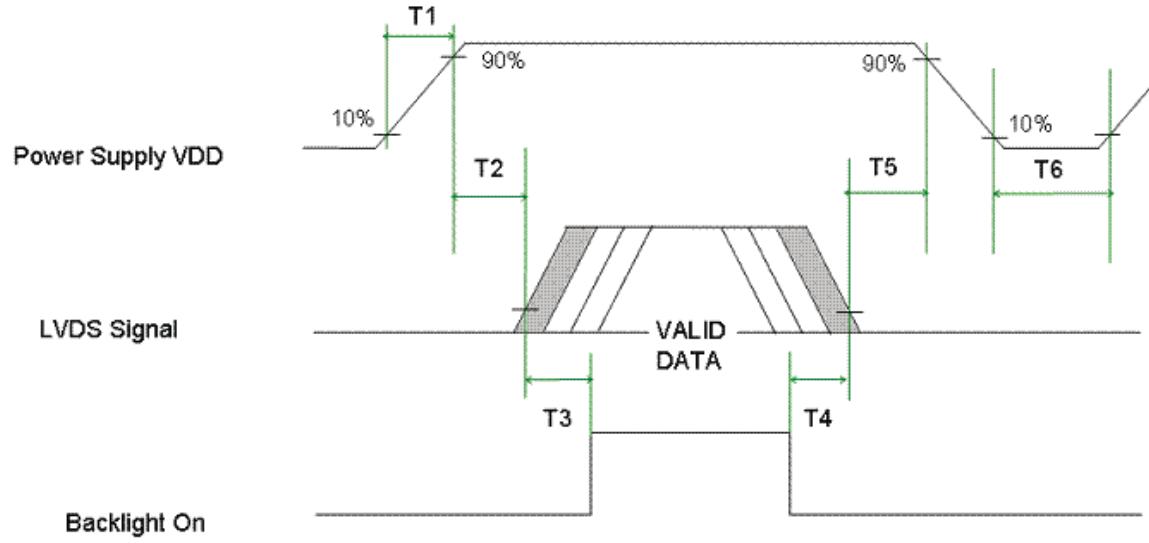
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6.6 Power ON/OFF Sequence

VDD power and backlight power on/off sequence are specified as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Parameter	Value		Unit
	Min.	Max.	
T1	0.5	10	[msec]
T2	0	50	[msec]
T3	500	-	[msec]
T4	200	-	[msec]
T5	0	50	[msec]
T6	1000	-	[msec]



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7 Connector and Pin Assignment

Physical interface is described as follows for the connector on open cell. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Open Cell

Connector Name / Designation	Interface Connector / Interface Card
Manufacturer	JAE P-TWO
Type Part Number	FI-XPB30SRLA-HF11 01-187121-30091-3(A)
Mating Housing Part Number	FI-X30HL (Locked Type)

7.1.1 LVDS Connector Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	GND	8	RxOCLKIN-
9	RxOCLKIN+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	GND
15	RxEIN1-	16	RxEIN1+
17	GND	18	RxEIN2-
19	RxEIN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	RxEIN3+	24	GND
25	NC (for AUO test only. Do not connect)	26	NC (for AUO test only. Do not connect)
27	NC (for AUO test only. Do not connect)	28	VDD
29	VDD	30	VDD



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8 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50 °C, 80%RH, 300 hours	
High Temperature Operation (HTO)	Ta= 50 °C, 50%RH, 300 hours	
Low Temperature Operation (LTO)	Ta= 0 °C, 300 hours	
High Temperature Storage (HTS)	Ta= 60 °C, 300 hours	
Low Temperature Storage (LTS)	Ta= -20 °C, 300 hours	
Thermal Shock Test (TST)	-20 °C/30min, 60 °C/30min, 100 cycles	Note 1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 15 points, 25 times/ point	Note 2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 15 points, 25 times/ point	

Note 1: The TFT-LCD Open Cell will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20 °C to 60 °C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed:

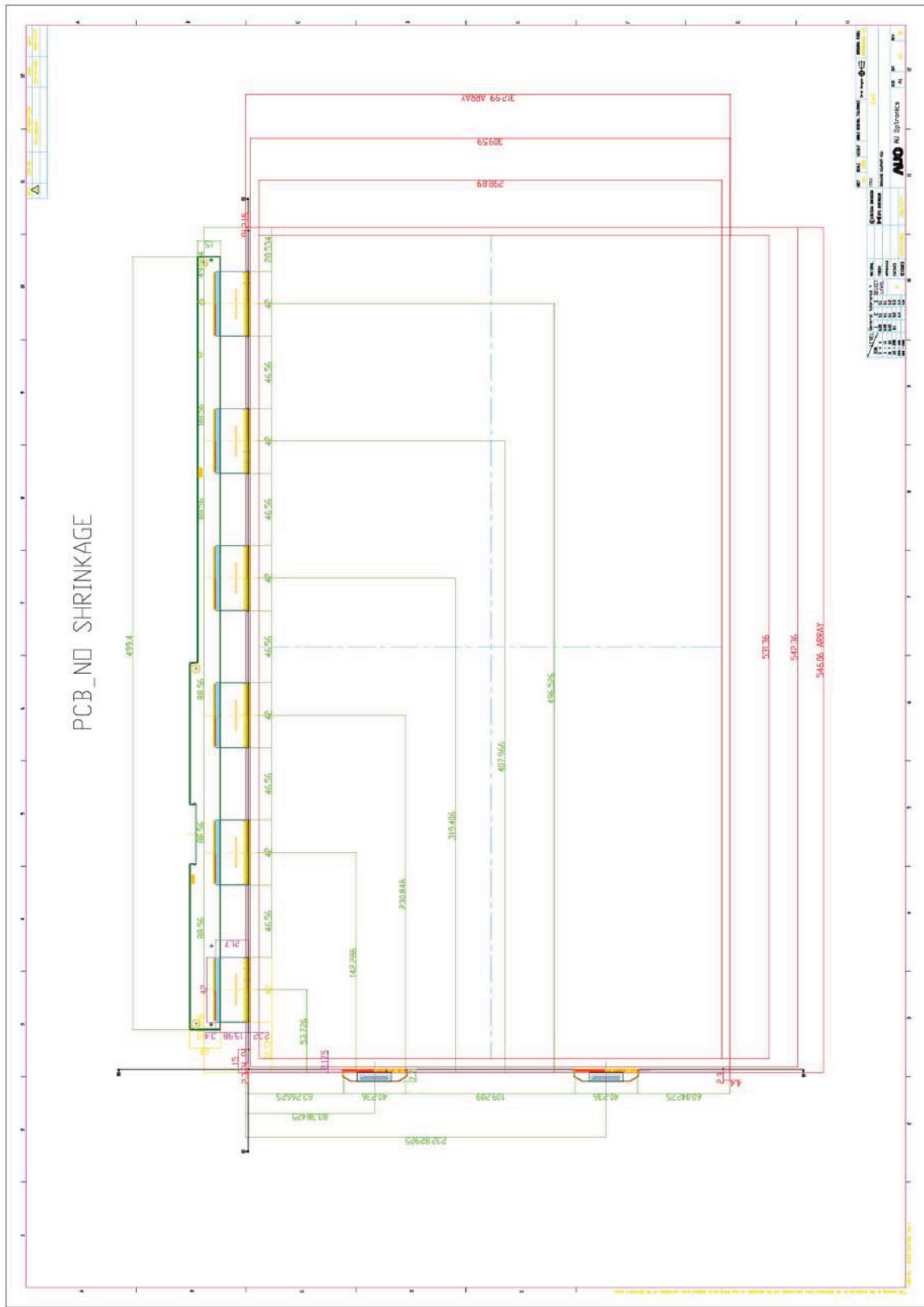
- No data lost
- Self-recoverable
- No hardware failures



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9 Mechanical Characteristics





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